CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model : CT62M6432A _ - _ _

Revision	00
Engineering	Jackson Fung
Date	20 May 2015
Our Reference	

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TFT NUMBER NOTATION:

C T 62 M 6432 A N - 00

| | | | | | | |

(1)(2)(3)(4) (5) (6) (7) (8)

*(1)--- C for Clover

*(2)--- T for TFT

*(3)--- Module size
- 35 – 3.5”
- 43 – 4.3”
- 50 – 5.0”
- 57 – 5.7”
- 62 – 6.2”
- 70 – 7.0”
- 10 – 10.0”

*(4)--- Display type
- M – Mono
- C – Color

*(5)--- Resolution

*(6)--- Model

*(7)--- Touch Panel
- N – No Touch Panel
- C – Capacitive Touch Panel
- D – Digital Key Touch Sensors
- R – Resistive Touch Panel

*(8)---Special code for other requirements

(Can be omitted if not used)

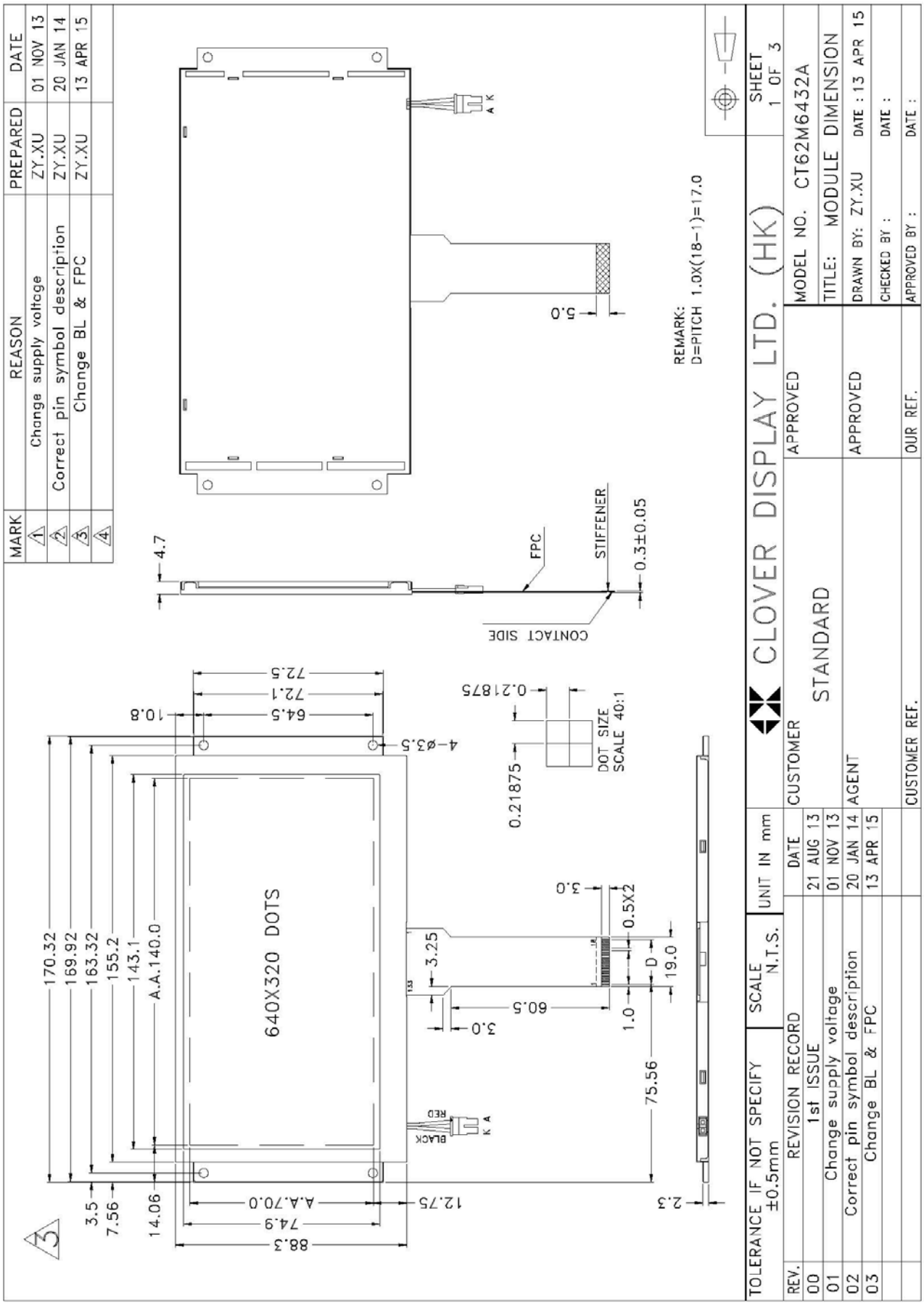
GENERAL DESCRIPTION

No.	Item	Specification	Unit
1	Panel Size	6.2”	Inch
2	Driver Element	a-Si TFT Active Matrix	Pixels
3	Number of Pixels	640 x 320	Pixels
4	Active Area	140(W) x 70(H)	mm
5	Pixel Pitch	0.21875(W) x 0.21875(H)	mm
6	Outline Dimension	170.32(W) x 88.3(H) x 4.7(D)	mm
7	Number of Colors	16, 4, 2 Gray Scale	
8	Display Mode	Normally Black VA / Transmmissive	
9	View Direction	6 O’clock	
10	Display Format	Mono Stripe Type	
11	Surface Treatment	–	
12	Contrast Ratio	800 (Typ)	
13	Luminance (cd/m^2)	750 (Typ)	cd/m^2
14	Interface	8 bit parallel / serial	
15	Backlight	White LED	
16	Weight	–	g

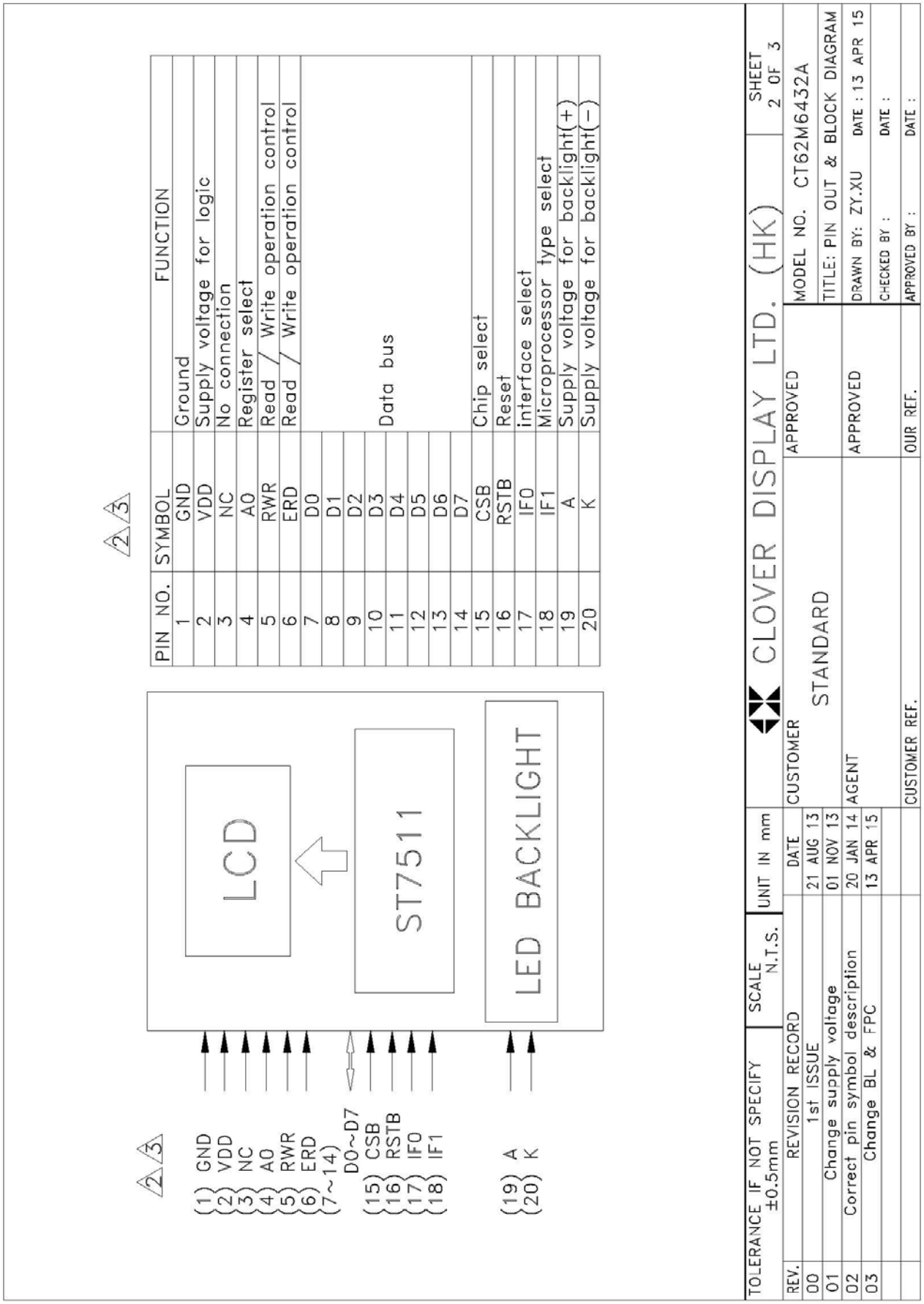
CONNECTOR PIN ASSIGNMENT

Pin No.	Symbol	Function
1	GND	Ground
2	VDD	Supply voltage for logic
3	NC	No connection
4	A0	Register select
5	RWR	Read / Write operation control
6	ERD	Read / Write operation control
7	D0	Data bus
8	D1	
9	D2	
10	D3	
11	D4	
12	D5	
13	D6	
14	D7	
15	CSB	Chip select
16	RSTB	Reset
17	IF0	Microprocessor type select
18	IF1	Interface select
19	K	Supply Voltage for Backlight (-)
20	A	Supply Voltage for Backlight (+)

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for Logic	VDD	4.75	5.0	5.25	V
Supply Current for Logic	IDD	—	15.0	22.5	μA
'High' Level Input Voltage	VIH	0.8VDD	—	—	V
'Low' Level Input Voltage	VIL	—	—	0.2VDD	V

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Side BL:
Constant voltage driving:

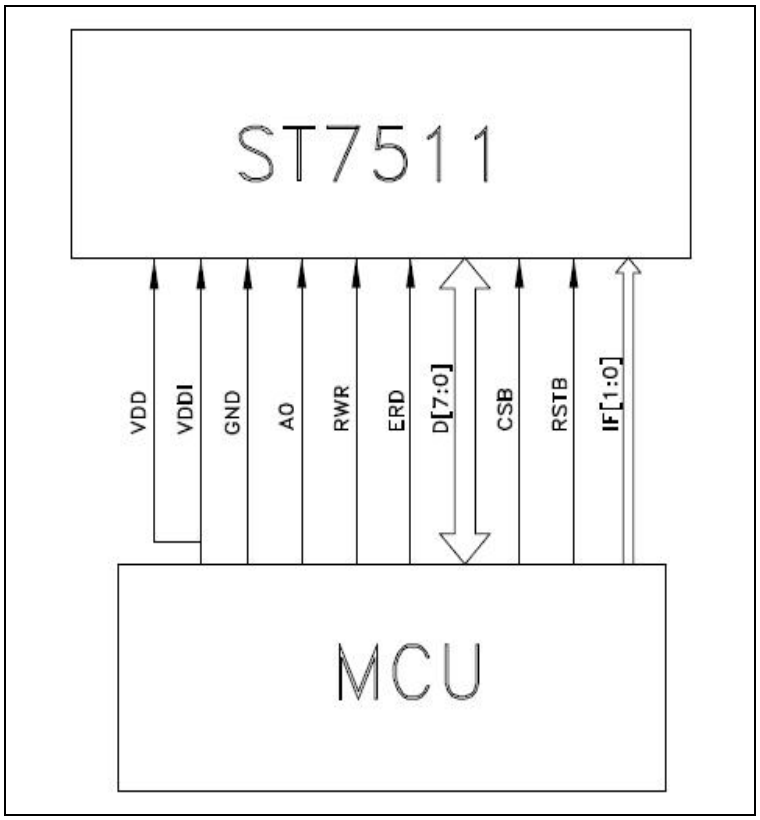
Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Backlight Voltage	V_{BL}	8.4	9.0	9.6	V	I_{BL} = 140 mA
Backlight Luminance	L_V	3000	—	—	cd/m^2	

ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3to6.0	V
Input Voltage	V_T	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opr}	-20 to 70	℃
Storage Temperature	T_{stg}	-30 to 80	℃
Humidity	—	90 MAX	% R.H.

REFERENCE CIRCUIT EXAMPLE



INSTRUCTIONS TABLE

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operation
		1	1	↑	1	0	1	0	0	1	0	1		
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display Invert Out
		1	1	↑	1	0	1	0	0	1	0	1		
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display Invert In
		1	1	↑	1	0	1	0	0	1	0	1		
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1		Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0		BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0		Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1		Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00	
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F	
		1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column

		1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00	Address Set
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00	
		1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02	
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F	
BLKFIL	29	0	1	↑	0	0	1	0	1	0	0	1		Block Fill
		1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BLSET	2B	0	1	↑	0	0	1	0	1	0	1	1		Blinking Set
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D	
		1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
WRRAM	2C	0	1	↑	0	0	1	0	1	1	0	0		Write RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
RDRAM	2D	0	1	↑	0	0	1	0	1	1	0	1		Read RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	X	X	X	X	X	X	X	X		
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
DISAR	31	0	1	↑	0	0	1	1	0	0	0	1		Display Area
		1	1	↑	0	0	0	0	0	0	0	DisLin8	01	
		1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F	
		1	1	↑	0	0	0	0	0	0	DisCol9	DisCol8	02	
		1	1	↑	DisCol7	DisCol6	DisCol5	DisCol4	DisCol3	DisCol2	DisCol1	DisCol0	7F	
DISSET1	32	0	1	↑	0	0	1	1	0	0	1	0		Display Set1
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32	
		1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02	
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00	
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01	
DISSET2	33	0	1	↑	0	0	1	1	0	0	1	1		Display Set2
		1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A	
		1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28	
		1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C	
		1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26	
PTLSET1	34	0	1	↑	0	0	1	1	0	1	0	0		Partial Set 1
		1	1	↑	0	0	0	0	0	0	0	Part1SL8	00	
		1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part1EL8	00	
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00	
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2
		1	1	↑	0	0	0	0	0	0	0	Part2SL8	00	
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00	

		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00	
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3
		1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00	
		1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	00	
		1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
VCMDAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00	
		1	1	↑	0	0	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00	
		1	1	↑	0	0	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00	
		1	1	↑	1	0	1	0	0	1	0	1		
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00	
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00	
		1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00	
		1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00	
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40	
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	01	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volumn Set 1
		1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A	
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06	
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volumn Set 2
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F	
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting
		1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44	
		1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44	
		1	1	↑	0	AVclClk_nd2	AVclClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44	

		1	1	↑	0	VgiClk_nd2	VgiClk_nd1	VgiClk_nd0	0	VghClk_nd2	VghClk_nd1	VghClk_nd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
		1	1	↑	ASLEDOf7	ASLEDOf6	ASLEDOf5	ASLEDOf4	ASLEDOf3	ASLEDOf2	ASLEDOf1	ASLEDOf0		
RDSTAT	72	0	1	↑	0	1	1	1	0	0	1	0		Read Status
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	0	0	0	0	0	R52	R51	R50		
		1	↑	1	0	R66	R65	R64	0	R62	R61	R60		
RDREV	73	0	1	↑	0	1	1	1	0	0	1	1		Read Revision
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
RDUID	75	0	1	↑	0	1	1	1	0	1	0	1		Read User ID
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60		
		1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70		
		1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80		
		1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90		
		1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0		
		1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
		1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	x	x	R15	R14	R13	R12	R11	R10		
		1	↑	1	x	x	R25	R24	R23	R22	R21	R20		
		1	↑	1	x	x	R35	R34	R33	R32	R31	R30		
		1	↑	1	x	x	R45	R44	R43	R42	R41	R40		
		1	↑	1	x	x	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	R65	R64	R63	R62	R61	R60		
		1	↑	1	x	x	R75	R74	R73	R72	R71	R70		

		1	↑	1	0	0	0	0	R83	R82	R81	R80		
GAMSET4 P1	91	0	1	↑	1	0	0	1	0	0	0	1		Gamma Set 4bpp Positive 1
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C	
GAMSET4 P2	92	0	1	↑	1	0	0	1	0	0	1	0		Gamma Set 4bpp Positive 2
		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4 P3	93	0	1	↑	1	0	0	1	0	0	1	1		Gamma Set 4bpp Positive 3
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4 P4	94	0	1	↑	1	0	0	1	0	1	0	0		Gamma Set 4bpp Positive 4
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2 P	95	0	1	↑	1	0	0	1	0	1	0	1		Gamma Set 2bpp Positive
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		Gamma Set 1bpp
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4 N1	99	0	1	↑	1	0	0	1	1	0	0	1		Gamma Set 4bpp Negative 1
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C	
GAMSET4 N2	9A	0	1	↑	1	0	0	1	1	0	1	0		Gamma Set 4bpp Negative 2
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	
		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4 N3	9B	0	1	↑	1	0	0	1	1	0	1	1		Gamma Set 4bpp Negative 3
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	

		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4 N4	9C	0	1	↑	1	0	0	1	1	1	0	0		Gamma Set 4bpp Negative 4
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2 N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set 2bpp Negative
		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify Write In
		1	1	↑	1	0	1	0	0	1	0	1		
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify Write Out
		1	1	↑	1	0	1	0	0	1	0	1		
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software Reset
		1	1	↑	1	0	1	0	0	1	0	1		

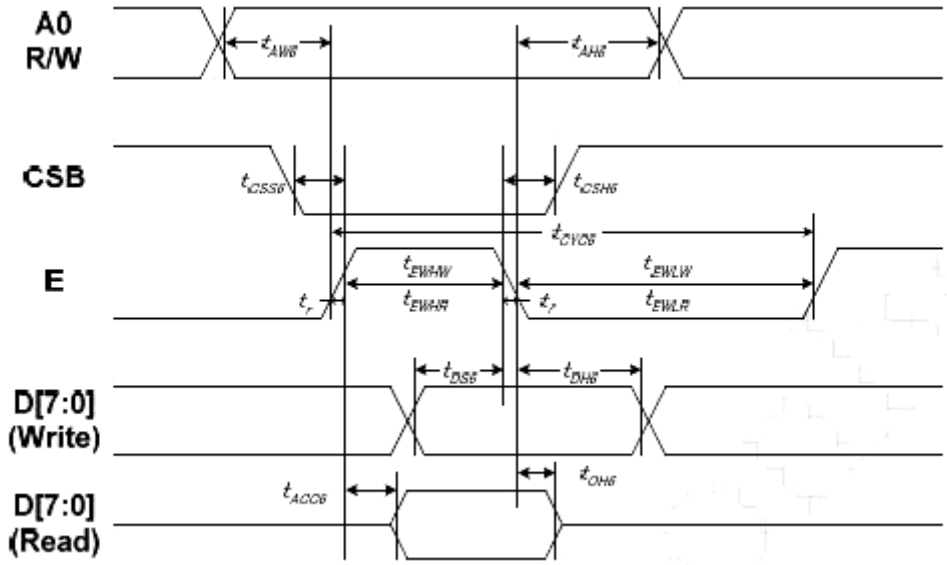
RECOMMENDED INITIAL SETTINGS

Software Reset：AEH,A5H
Power Control：61H,0FH,04H,02H,A5H
Electronic Volume Set 1：62H,00H,3BH,1BH,A5H
Electronic Volume Set 2：05H,0FH,3BH,A5H,A5H
Memory Address Control：24H,01H,A5H,A5H,A5H
BPP Select：22H,02H,A5H,A5H,A5H
Gamma Set 4bpp Positive 1：91H,00H,21H,23H,24H
Gamma Set 4bpp Positive 2：92H,27H,28H,29H,2AH
Gamma Set 4bpp Positive 3：93H,2BH,2CH,2DH,2EH
Gamma Set 4bpp Positive 4：94H,30H,31H,32H,3FH
Gamma Set 4bpp Negative 1：99H,00H,21H,23H,26H
Gamma Set 4bpp Negative 2：9AH,27H,28H,29H,2AH
Gamma Set 4bpp Negative 3：9BH,2BH,2CH,2DH,2EH
Gamma Set 4bpp Negative 4：9CH,30H,35H,3BH,35H
Sleep Out：12H,A5
Display On：15H,A5

DISPLAY DATA RAM

Page address		0	1	2	..	637	638	639	normal	Column address
normal	invert	639	638	637	..	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G0	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G1	
1	158	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G2	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G3	
:	:	:	:	:		:	:	:	:	
158	1	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G316	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G317	
159	0	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G318	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G319	
Source		S0	S1	S2	..	S637	S638	S639	Gate	

6800 SERIES PARALLEL INTERFACE TIMING DIAGRAM

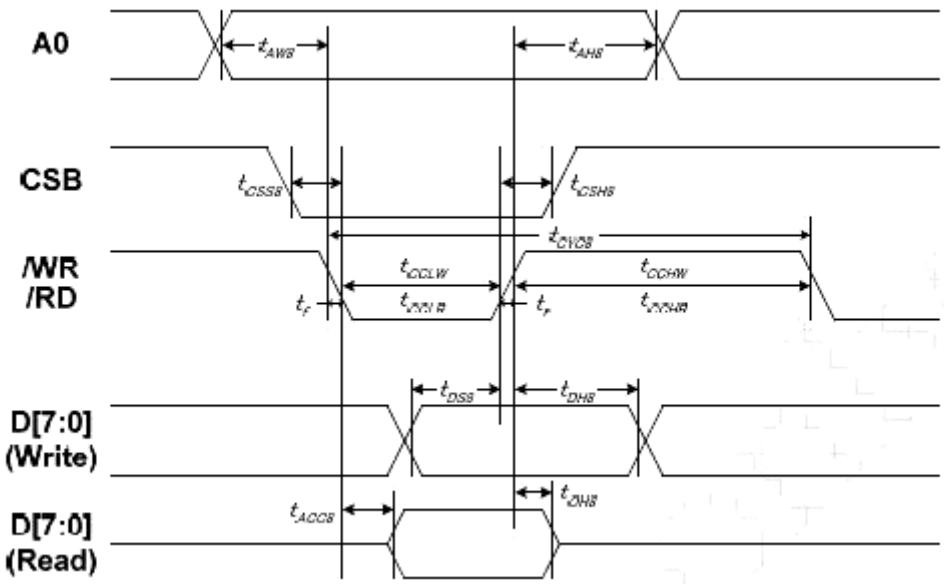


6800 SERIES PARALLEL INTERFACE TIMING CHARACTERISTICS

AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		1100	—	
Enable L pulse width (WRITE)		tEWLW		500	—	
Enable H pulse width (WRITE)		tEWHW		500	—	
Enable L pulse width (READ)		tEWLR		500	—	
Enable H pulse width (READ)		tEWHR		500	—	
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		130	—	
Write data setup time	D[7:0]	tDS6		200	—	
Write data hold time		tDH6		250	—	
Read data access time		tACC6	CL = 100 pF	—	950	
Read data output disable time		tOH6	CL = 100 pF	5	200	

8080 SERIES PARALLEL INTERFACE TIMING DIAGRAM

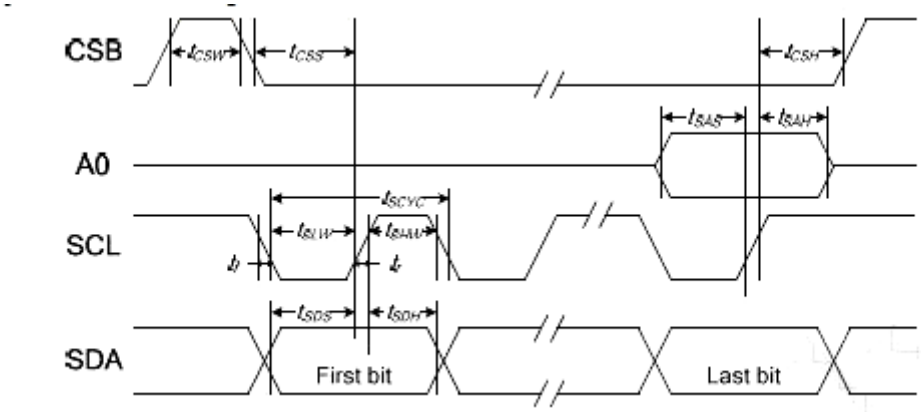


8080 SERIES PARALLEL INTERFACE TIMING CHARACTERISTICS

AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		1100	—	
/WR L pulse width (WRITE)		tCCLW		500	—	
/WR H pulse width (WRITE)		tCCHW		500	—	
/RD L pulse width (READ)	/RD	tCCLR		950	—	
/RD H pulse width (READ)		tCCHR		500	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		200	—	
WRITE Data hold time		tDH8		50	—	
READ access time		tACC8	CL = 100 pF	—	950	
READ Output disable time		tOH8	CL = 100 pF	5	200	

4-LINE SERIAL INTERFACE TIMING DIAGRAM

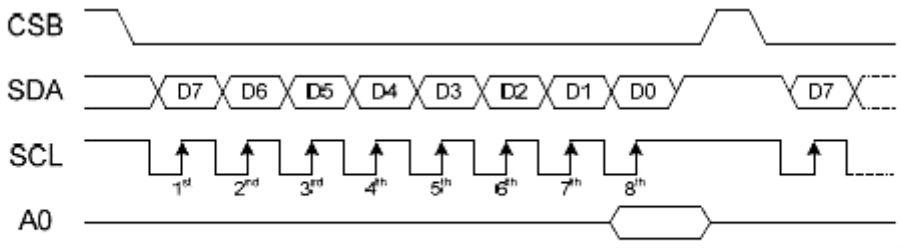


4-LINE SERIAL INTERFACE TIMING CHARACTERISTICS

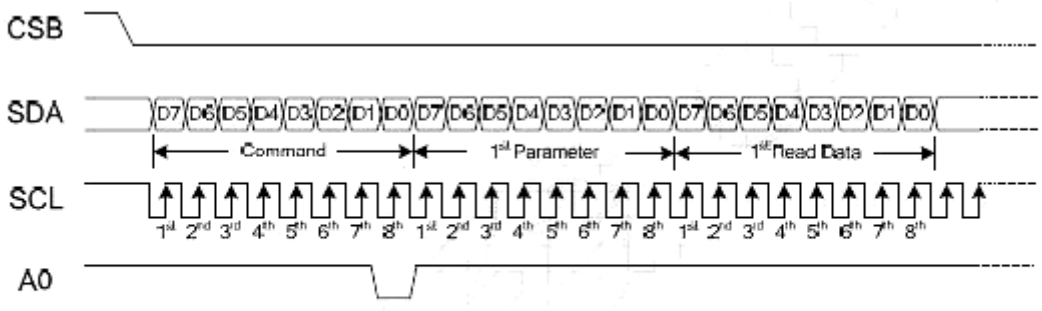
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		300	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Address setup time	A0	tSAS		150	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time		tSDH		120	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

4-LINE SPI MODE DIAGRAM

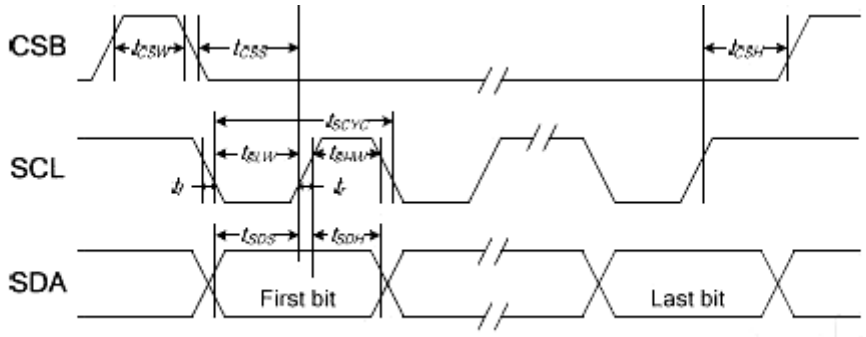


Write-Operation of 4-Line Serial Interface



Read-Operation of 4-Line Serial Interface

3-LINE SERIAL INTERFACE TIMING DIAGRAM



3-LINE SERIAL INTERFACE TIMING CHARACTERISTICS

AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time		tSDH		120	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

3-LINE SPI MODE DIAGRAM

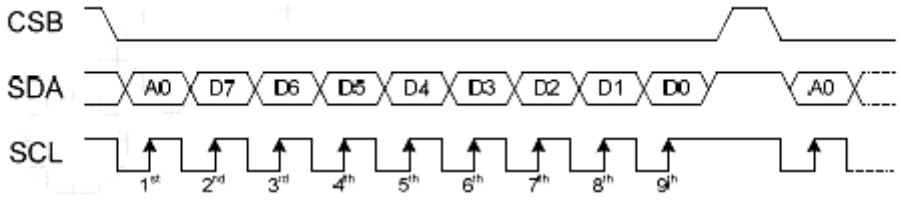
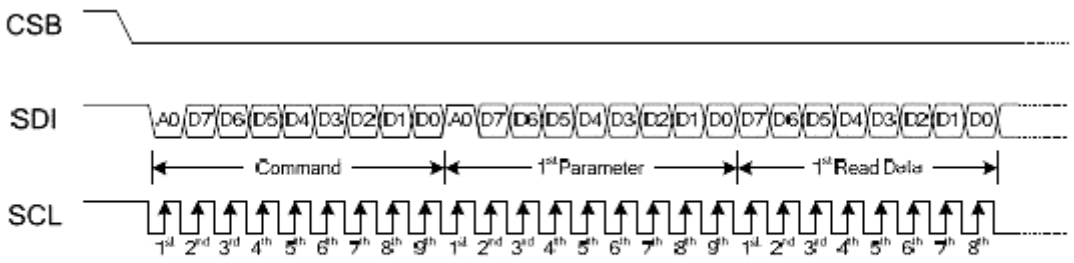
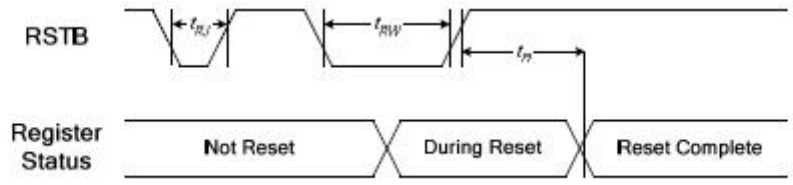


Fig 3 Write-Operation of 3-Line Serial Interface



Read-Operation of 3-Line Serial Interface

RESET TIMING DIAGRAM



RESET TIMING

AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 *1	us
Reset "L" pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns

THE RESET OF CIRCUIT

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating.

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = V_{OP} / 64 Hz
TEMPERATURE = 23 ± 5 °C
RELATIVE HUMIDITY = 50 ± 20 %

ITEM	SYMBOL	UNIT	Value
RESPONSE TIME	Ton	ms	20
	Toff	ms	10
CONTRAST RATIO	Cr	-	800
VIEWING ANGLE (6 O'clock) Cr ≥ 2	V3:00	°	60
	V6:00	°	50
	V9:00	°	60
	V12:00	°	60

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

NO.	Item	TEST CONDITION FOR WIDE TEMPERATURE	TIME
1	High Temperature Storage	80°C	240 hours
2	Low Temperature Storage	-30°C	240 hours
3	High Temperature Operation	70°C	240 hours
4	Low Temperature Operation	-20°C	240 hours
5	High Temperature Humidity Storage	60°C, 90%RH	240 hours
6	Thermal Shock Non - Operating	-30°C/1hr ~ +80°C/1 hr for a total 100 cycles	100 cycle
7	Vibration Test	Frequency range : 10~55Hz Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz	2 hours for each direction of X. Y. Z. (6 hours for total)
8	Package Drop Test	Height : 60cm 1 corner, 3 edges, 6 surfaces	—
9	Electro Static Discharge	+/-2KV, Human Body Mode, 100pF/1500Ω	—

Note 1: Test after 24 hours in room temperature (25+/-5°C).
Note 2: The sampling above is individually for each reliability testing condition.
Note 3: The color fading of polarizing filter should not care.
Note 4: All of the reliability testing chamber above, is using D.I. water. (Min value : 1.0MΩ-cm).

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

THE ENVIRONMENTAL CONDITION OF INSPECTION

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature : 25+/-5°C
(2) Humidity : 25-75 % RH
(3) Panel visual inspection on the operation condition for cosmetic shall be conducted at the distance 30~40cm or more between the LCD module and eyes of inspector.
Ambient Illumination : 800~1200 Lux for external appearance inspection
Ambient Illumination : 200~500 Lux for light on inspection
(4) The viewing angel:
a) +/-15 degree to the front surface of display panel in vertical direction.
b) +/-15 degree to the front surface of display panel in horizontal direction.

INSPECTION CRITERIA

(1) Definition of dot defect induced from the panel inside
a) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
b) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.
c) 2 dot adjacent = 1 pair = 2dots

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING

- The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.
- To avoid contamination on the display surface, do not touch the module surface with bare hands.
- Keep a space so that the LCD panels do not touch other components.
- Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.
- Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.
- Do not leave module in direct sunlight to avoid malfunction of the ICs.

(2) CAUTION OF LCD CLEANING

- Do not wipe the polarizer with dry cloth. It might cause scratch.
- Only use a soft cloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

(3) CAUTION OF STORAGE

- Store the module in a dark room where must keep at 25+/-10°C and 65%RH or less.
- Do not store the module in surroundings containing organic solvent or corrosive gas.
- Store the module in an anti-electrostatic container or bag.

(4) STATIC ELECTRICITY

- Be sure to ground module before turning on power or operating module.
- Do not apply voltage which exceeds the absolute maximum rating value.

(5) TRANSPORTATION PRECAUTIONS

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

(6) SAFETY

- For crash damage or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.
- When any liquid leaked out of a damage glass cell comes in contact with your hands, wash it off with soap and water.