

ZETTLER DISPLAYS

XIAMEN ZETTLER ELECTRONICS CO., LTD.

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

CUSTOMER APPROVAL			
※ PART NO. : <u>AQM0802A-RN-GBW (ZETTLER DISPLAYS) VER1.0</u>			
APPROVAL		COMPANY CHOP	
CUSTOMER COMMENTS			

ZETTLER DISPLAYS ENGINEERING APPROVAL		
DESIGNED BY	CHECKED BY	APPROVED BY
SDF	LIUH	GU ZH

REVISION RECORD

REVISION	REVISION DATE	PAGE	CONTENTS
VER1.0	2014-03-06		FIRST ISSUE

※ **CONTENTS**

- 1.0 GENERAL PECS
- 2.0 ABSOLUTE MAXIMUM RATINGS
- 3.0 ELECTRICAL CHARACTERISTICS
- 4.0 OPTICAL CHARACTERISTICS
- 5.0 BLOCK DIAGRAM
- 6.0 PIN ASSIGNMENT
- 7.0 POWER SUPPLY
- 8.0 TIMING CHARACTERISTICS
- 9.0 MECHANICAL DIAGRAM
- 10.0 RELIABILITY TEST
- 11.0 DISPLAY INSTRUCTION TABLE
- 12.0 I2C INTERFACE
- 13.0 STANDARD CHARACTER PATTERNS
- 14.0 APPEARANCE CRITERIA
- 15.0 PRECAUTION FOR USING LCM

1.0 GENERAL SPECS

1. Display Format	8*2 Character
2. Power Supply	3.3V
3. Overall Module Size	30.0mm(W) x 19.5mm(H) x max1.8mm(D)
1. Viewing Area(W*H)	27.0mm(W) x 10.5mm(H)
1. Dot Size (W*H)	0.45mm(W) x 0.50mm(H)
2. Dot Pitch (W*H)	0.50mm(W) x 0.55mm(H)
3. Character Size (W*H)	2.45mm(W) x 4.35mm(H)
4. Character Pitch (W*H)	2.95mm(W) x 4.90mm(H)
5. Viewing Direction	6:00 O'Clock
6. Driving Method	1/16Duty,1/5Bias
7. Controller IC	ST7032I-0D or compatible
1. Display Mode	STN(Gray)/Positive/Reflective
1. Backlight Options	NC
1. Operating temperature	-20°C ~ 70°C
1. Storage temperature	-30°C ~ 80°C
2. RoHS	RoHS Compliant

2.0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Typ	Max	Unit
Operating temperature	Top	-20	-	70	°C
Storage temperature	Tst	-30	-	80	°C
Input voltage	Vin	Vss	--	Vdd	V
Supply voltage for logic	Vdd- Vss	2.7	-	5.5	V
Supply voltage for LCD drive	Vdd- Vo	3.0	-	7.0	V

3.0 ELECTRICAL CHARACTERISTICS

3.1 Electrical Characteristics Of LCM

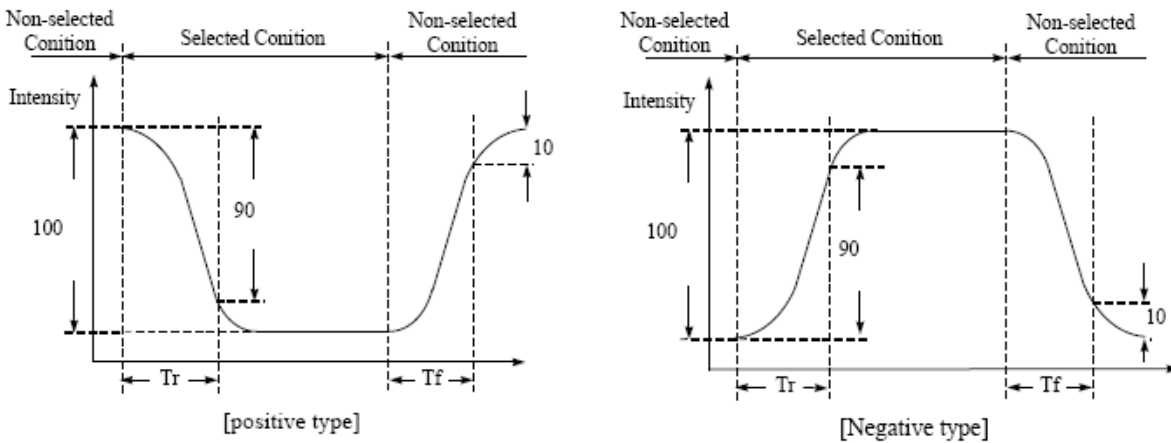
Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	Vdd	25°C	3.1	3.3	3.5	V
Power Supply Current	Idd	Vdd=3.3V	--	0.5	1.0	mA
Input voltage (high)	Vih	Pins:(SDA,SCL,XRS ETB),Vdd=3.3V	0.8Vdd	--	Vdd	V
Input voltage (low)	Vil		0	--	0.2Vdd	V
Recommended Driving Voltage	LC	Vdd -Vo	-20°C	--	5.0	V
			25°C	--	4.5	
			70°C	4.0	--	

3.2 The Characteristics Of LED Backlight(NC)

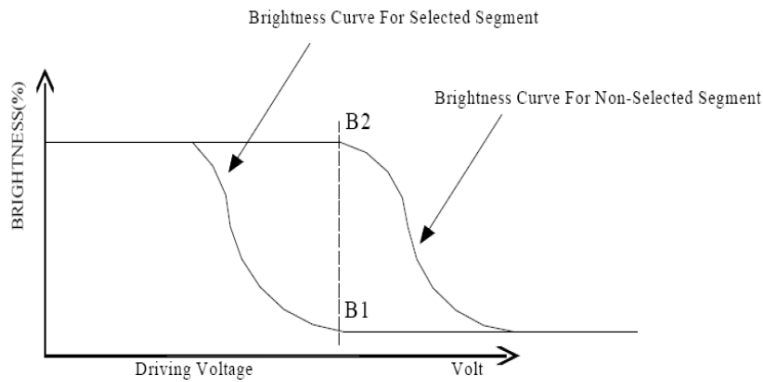
4.0 OPTICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Viewing angle (Left - right)	θ_2	$Cr \geq 2.0$	-35	-	35	deg
Viewing angle (Up-down)	θ_1	$Cr \geq 2.0$	-20	-	35	deg
Contrast Ratio	Cr	$\theta_1=0^\circ, \theta_2=0^\circ$	-	6	-	
Response time (rise)	Tr	$\theta_1=0^\circ, \theta_2=0^\circ$	-	180	300	ms
Response time (fall)	Tf	$\theta_1=0^\circ, \theta_2=0^\circ$	-	150	250	ms

(1). Definition of Optical Response Time

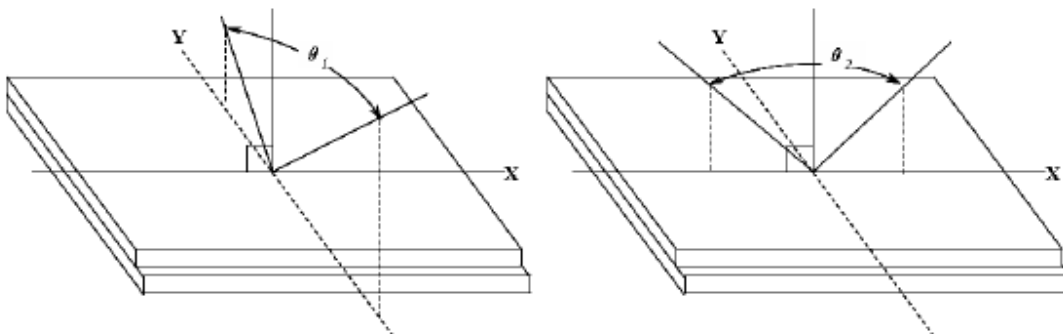


(2). Definition of Contrast Ratio

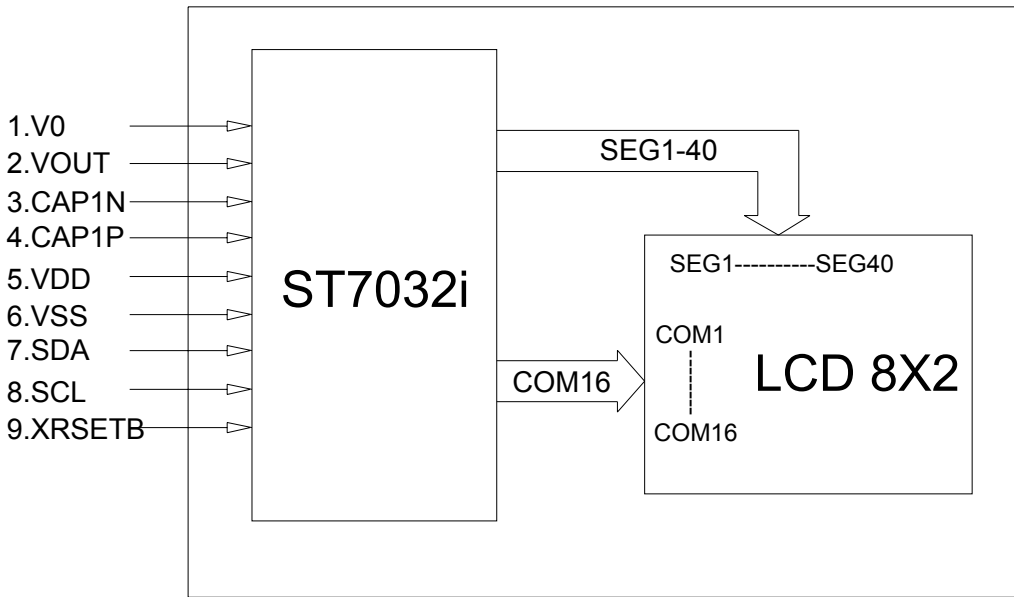


$$Cr = \frac{\text{Brightness of Non-selected Segment}(B2)}{\text{Brightness of selected Segment}(B1)}$$

(3). Definition of Viewing Angle θ_2 and θ_1



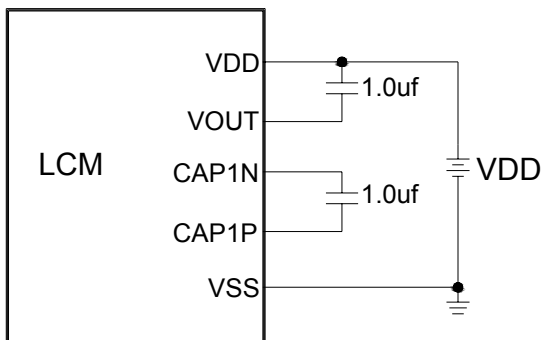
5.0 BLOCK DIAGRAM



6.0 PIN ASSIGNMENT

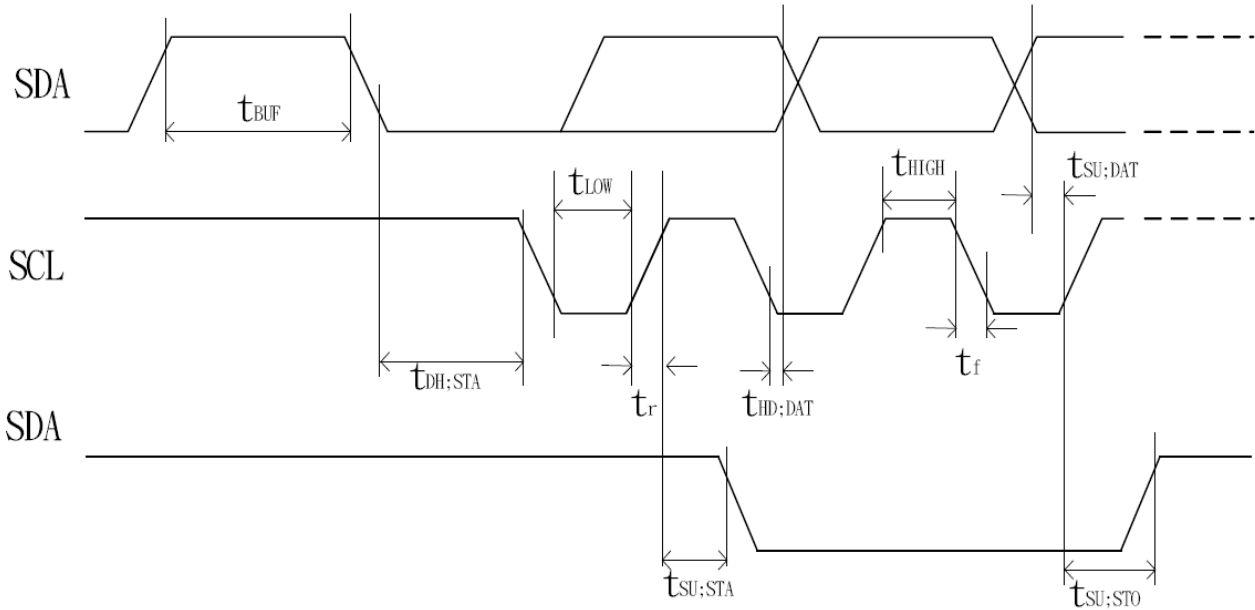
Pin No.	Symbol	Function
1	VO	Test PIN for VLCD,leave it open
2	VOUT	DC/DC voltage converter output
3	CAPIN	For voltage booster circuit(VDD-VSS) External capacitor about 0.1u~4.7uf
4	CAPIP	
5	VDD	+3.3V
6	VSS	Ground
7	SDA	Serial data input
8	SCL	Serial clock input
9	XRSETB	Chip reset signal. Active when low

7.0 POWER SUPPLY



8.0 TIMING CHARACTERISTICS

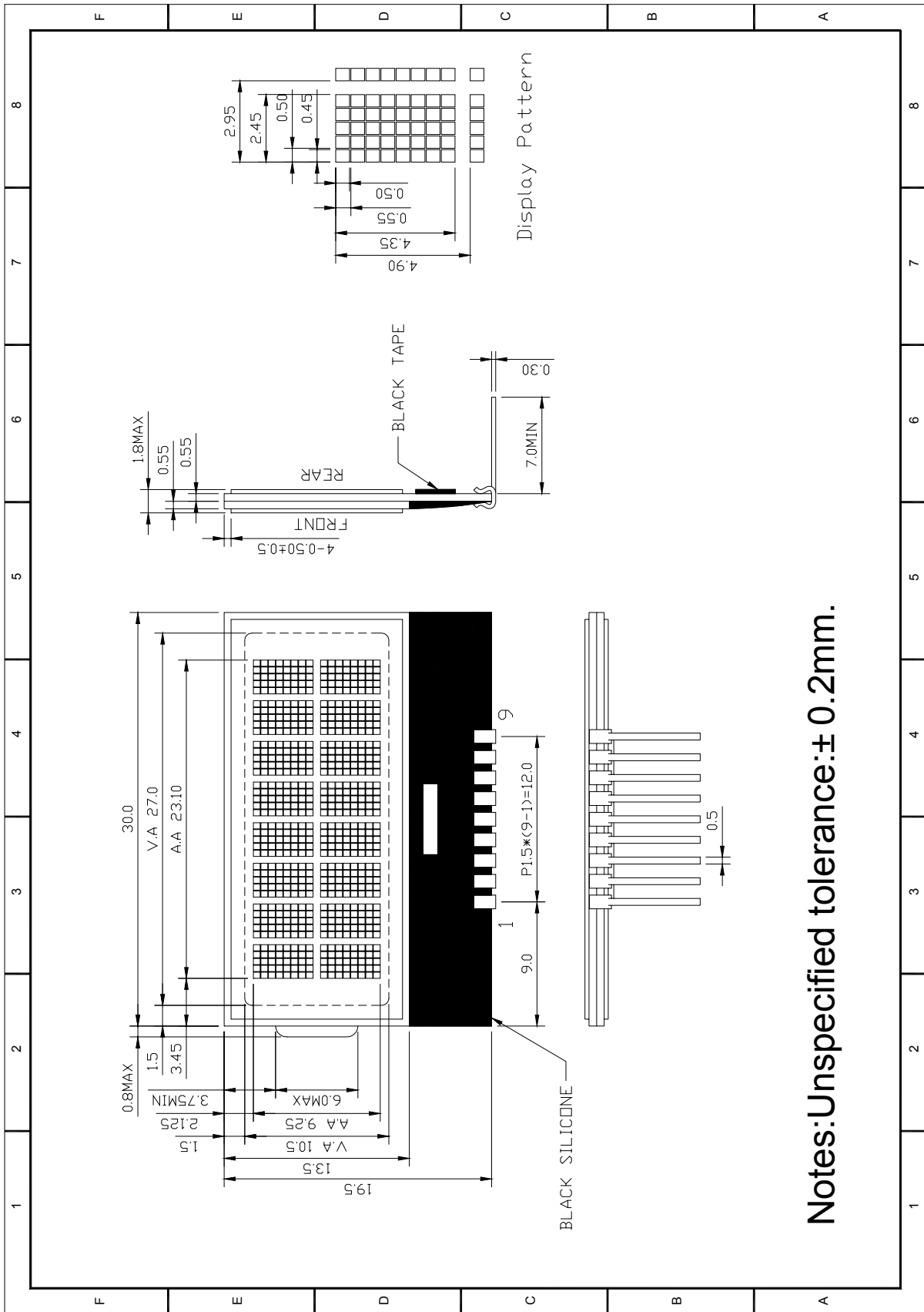
- I2C interface



(Ta = -30°C to 85°C)

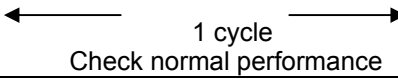
Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}	—	1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}	—	0.6	—	0.6	—	us
Data set-up time	SI	$t_{SU;DAT}$	—	180	—	100	—	ns
Data hold time		$t_{HD;DAT}$	—	0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	$20+0.1C_b$	300	$20+0.1C_b$	300	ns
SCL,SDA fall time		t_f	—	$20+0.1C_b$	300	$20+0.1C_b$	300	
Capacitive load represent by each bus line		C_b	—	—	400	—	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.6	—	0.6	—	us
Start condition hold time		$t_{HD;STA}$	—	0.6	—	0.6	—	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	—	0.6	—	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	—	1.3	—	us

9.0 MECHANICAL DIAGRAM



Notes: Unspecified tolerance: ± 0.2mm.

10.0 RELIABILITY TEST

NO	Test Item	Description	Test Condition	Remark	
1	Environmental Test	High temperature storage	Applying the high storage temperature Under normal humidity for a long time Check normal performance	80 °C 96hrs	
2		Low temperature storage	Applying the low storage temperature Under normal humidity for a long time Check normal performance	-30°C 96hrs	
3		High temperature Operation	Apply the electric stress(Volatge and current) Under high temperature for a long time	70 °C 96hrs	Note1
4		Low temperature Operation	Apply the electric stress Under low temperature for a long time	-20°C 96hrs	Note1 Note2
5		High temperature/High Humidity Storage	Apply high temperature and high humidity storage for a long time	90% RH 40°C 96hrs	Note2
6		Temperature Cycle	Apply the low and high temperature cycle -30°C <> 25°C <> 80°C <> 25°C 30min 10min 30min 10min  1 cycle Check normal performance	-30°C/80°C 10 cycle	
7	Mechanical Test	Vibration test(Package state)	Applying vibration to product check normal performance	Freq:10-55Hz Max Acceleration 5G 1cycle time:1min time X.Y.Z direction for 15 mines	
8		Shock test(package state)	Applying shock to product check normal performance	Drop them through 70cm height to strike horizontal plane	
9	Other				

Remark

Note1:Normal operations condition (25°C±5°C).

Note2:Pay attention to keep dewdrops from the module during this test.

11.0 DISPLAY INSTRUCTION TABLE

➤ instruction table at “Extension mode”

(when “EXT” option pin connect to Vss, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540KHz	OSC=700KHz	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms	
Return Home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us	
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us	
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0	
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us	
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us	

Note *: this bit is for test command , and must always set to "0"

Instruction table 0(IS=0)

Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

Instruction table 1(IS=1)

Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab2	Rab1	Rab0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

12.0 I2C INTERFACE

**It just only could write Data or Instruction to ST7032 by the IIC Interface.
It could not read Data or Instruction from ST7032 (except Acknowledge signal).**

SCL: serial clock input

SDA: serial data input

Slaver address could only set to 0111110, no other slaver address could be set

The I C interface send RAM data and executes the commands sent via the I C Interface. It could send data bit to the RAM. The I C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA)

and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.1.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.3.

·Transmitter: the device, which sends the data to the bus

·Master: the device, which initiates a transfer, generates clock signals and terminates a transfer-Slave: the device addressed by a master

Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

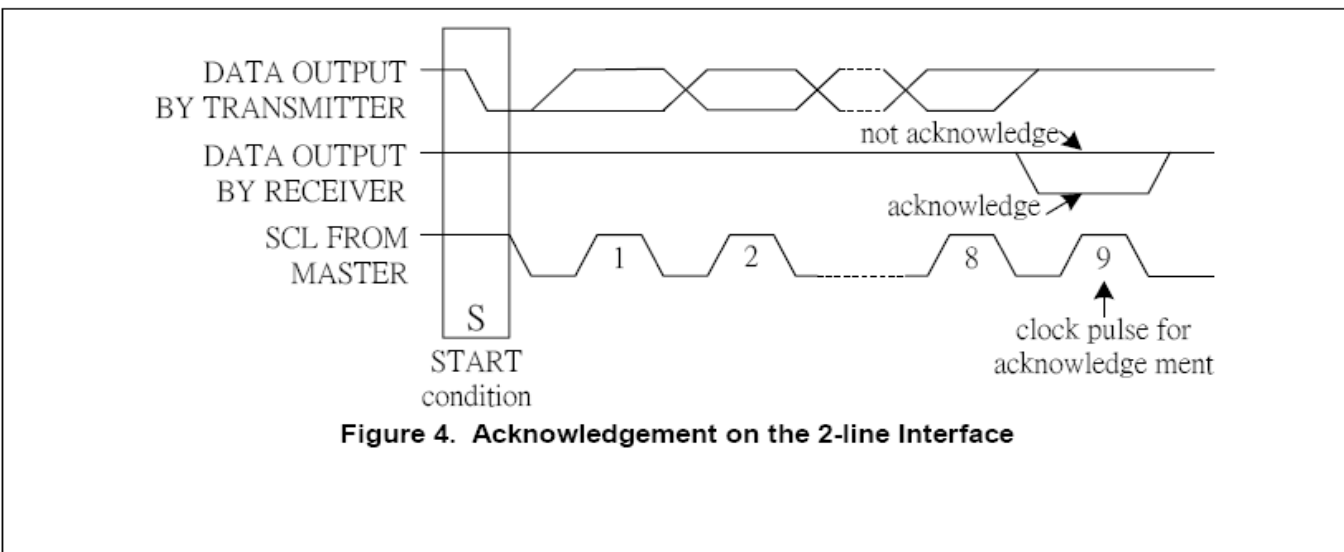
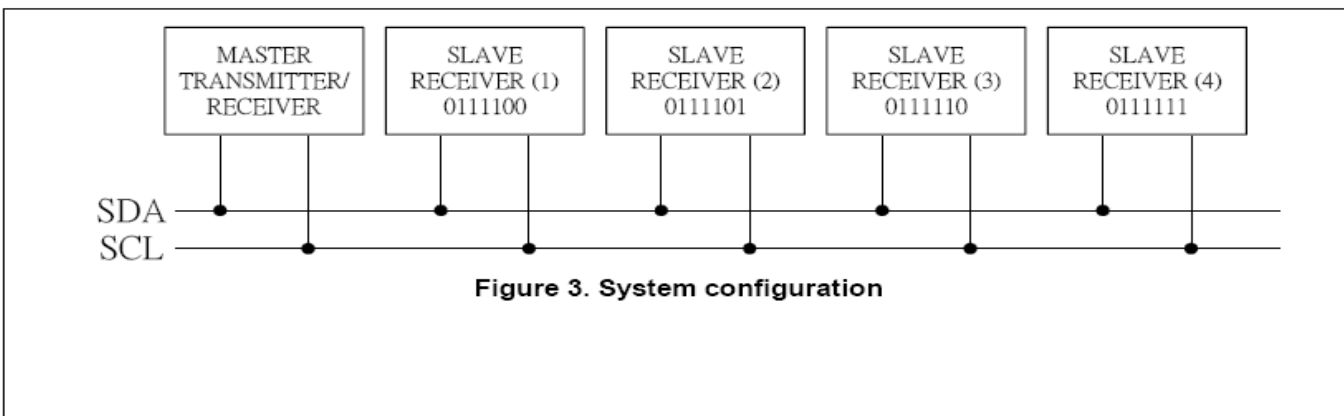
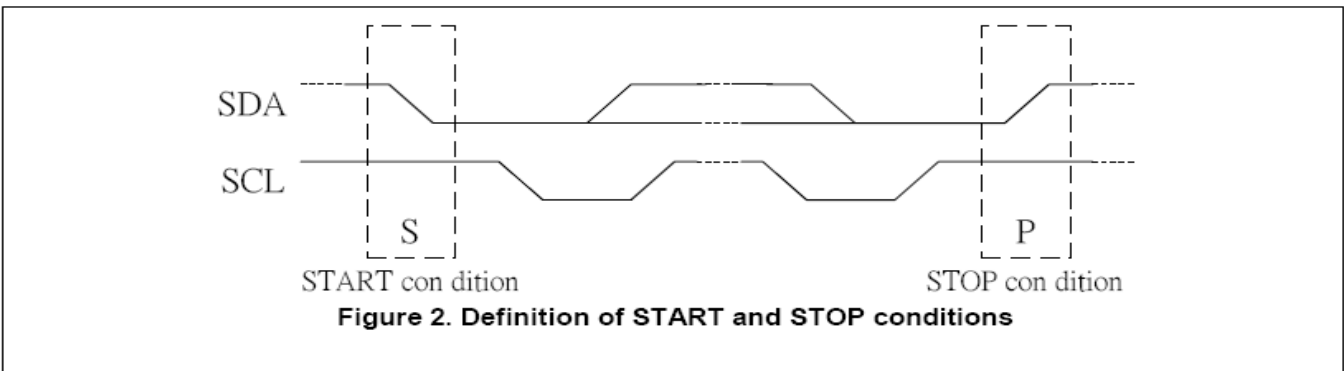
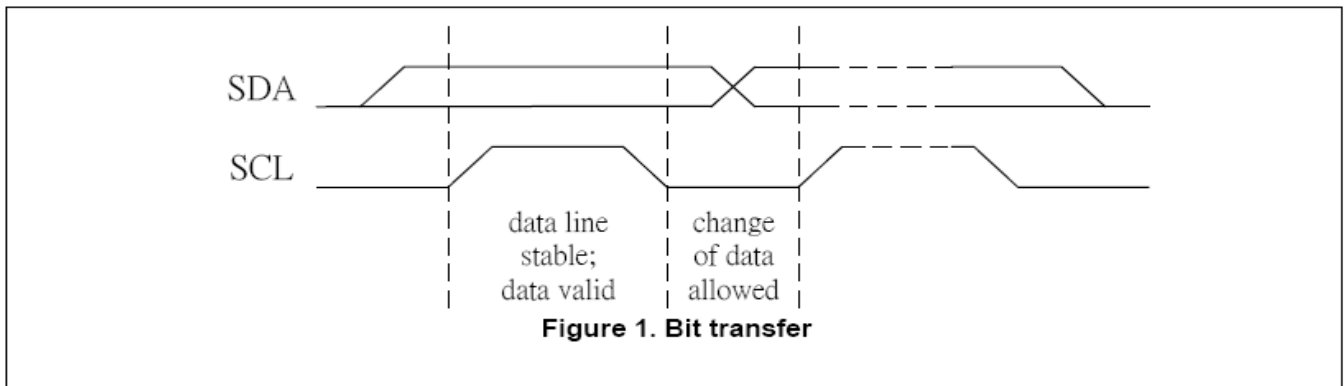
·Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

·Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Acknowledge is not Busy Flag in I2C interface.

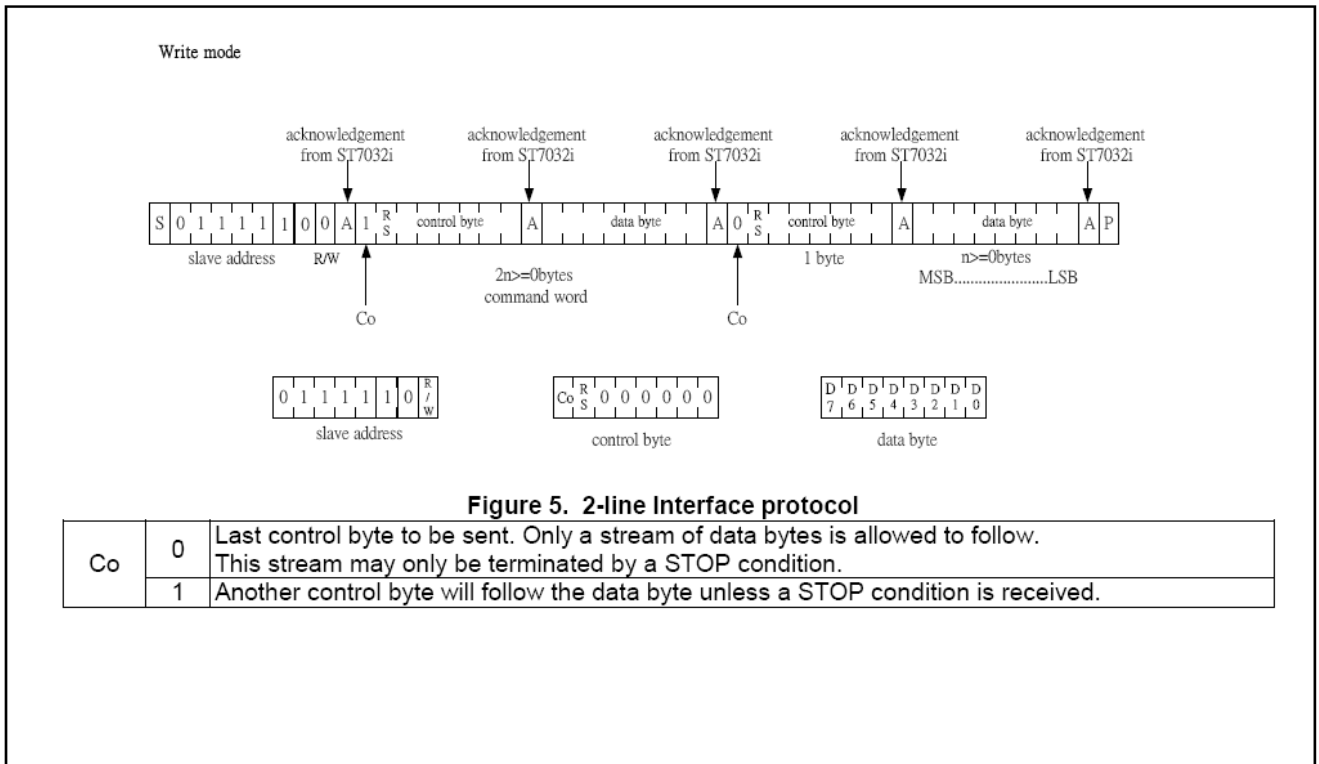
Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I C Interface is illustrated in Fig.4.



I2C Interface protocol

The ST7032 supports command, data write addressed slaves on the bus
 Before any data is transmitted on the I C Interface, the device, which should respond, is addressed first. Only one 7-bit slave addresses (0111110) is reserved for the ST7032. The R/W is assigned to 0 for Write only.
 The I C Interface protocol is illustrated in Fig.5.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and RS, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7032i device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C INTERFACE-bus master issues a STOP condition (P).



During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR)

The data register (DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input in I C interface.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

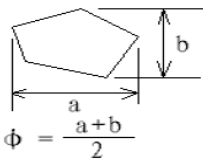
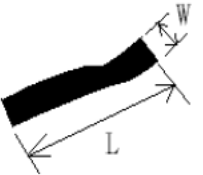
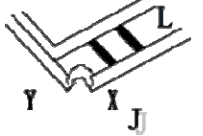
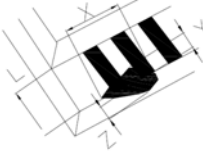
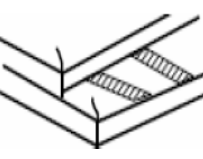

Table 2. Various kinds of operations according to RS and R/W bits.

13.0 STANDARD CHARACTER PATTERNS

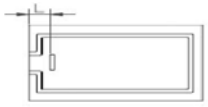
ST7032-0D (ITO option OPR1=1, OPR2=1)

b7-b4 b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	!	@	#	\$	%	&	'	()	*	+	=	>	<	?	~
0001	J	T	!	l	A	Q	a	W	Q	e	w	7	7	△	△	~
0010	@	S	"	2	B	R	b	r	é	É	T	t	U	u	△	△
0011	P	7	#	3	C	S	c	s	À	à	¡	í	É	é	Ü	ü
0100	4	7	\$	4	D	T	d	t	á	á	¢	¢	É	É	Ü	Ü
0101	†	Δ	×	5	E	U	e	u	â	â	£	£	É	É	Ü	Ü
0110	↓	θ	×	6	F	V	f	v	ã	ã	¥	¥	É	É	Ü	Ü
0111	→	Δ	^	7	G	W	g	w	ä	ä	¥	¥	É	É	Ü	Ü
1000	+	Ξ	∞	8	H	X	h	x	å	å	¥	¥	É	É	Ü	Ü
1001	∞	∞	>	9	I	Y	i	y	æ	æ	∞	∞	É	É	Ü	Ü
1010	∞	∞	*	*	J	Z	j	z	æ	æ	∞	∞	É	É	Ü	Ü
1011	L	∞	+	*	K	L	k	l	ï	ï	∞	∞	É	É	Ü	Ü
1100	U	∞	*	<	L	∞	l	l	ï	ï	∞	∞	É	É	Ü	Ü
1101	*	∞	-	=	N	∞	n	>	ï	ï	∞	∞	É	É	Ü	Ü
1110	∞	∞	.	>	N	∞	n	>	∞	∞	∞	∞	É	É	Ü	Ü
1111	∞	∞	/	?	∞	∞	∞	∞	∞	∞	∞	∞	É	É	Ü	Ü

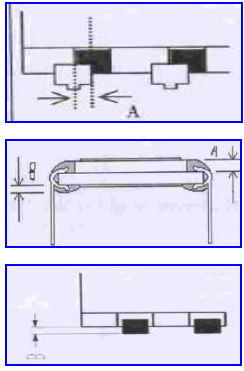
14.0 APPEARANCE CRITERIA

Item	Description	Picture	Specification			MA	MI	Inspection Method
Dot defects (black/white dot)	Scratches black dot white dot on the polarizer dirty spot and bubble between the polarizer and glass in the display area.	 <p>J:the distance between dot and dot.</p>	≤ 0.1	Ignored		●		Visual/contrast by Inspection standard film
			$0.1 < \phi \leq 0.20$	2	$J > 5$			
			$0.20 < \phi \leq 0.25$	1	$J > 10$			
			$0.25 < \phi \leq 0.30$	0				
			$0\phi > 0.3$	0				
black/white line defect (straight line or curve etc. Line type defects)	Fibres in active area, scratches and black line on the glass or polarizer.	 <p>J:the distance between dot and dot.</p>	$W \leq 0.01$	Ignored		●		Visual/contrast by Inspection standard film
			$W \leq 0.02 \quad L \leq 5$	2	$J > 5$			
			$W \leq 0.03 \quad L \leq 4$	1	$J > 10$			
			$W \leq 0.04 \quad L \leq 3$	0	$J > 10$			
			$W \leq 0.05 \quad L \leq 2$	0				
Chip on corner	sidestep on the lower glass	 <p>Y:width of chip X:length of chip L:width of sidestep J:distance between electrode and the farthest edge.</p>	$Y \leq 1/2L, X \leq 1$	Ignored		●		Visual/contrast by Inspection standard film
			$Y \leq 1/2L, X \leq 2$	2				
			$Y \leq 1/2L, X \leq 3$	1				
			$Y \leq 1/2L, X \leq 1/3J$	0	$J \leq 3$			
			$Y \leq 1/2L, X \leq 2/3J$	0	$J \leq 3$			
Crack		 <p>Y:width of crack X:length of crack L:width of sidestep T:depth of crack Z:thickness of single glass</p>	$Y \leq 1/5L \quad X \leq 5 \quad Z \leq 1/2T$	Ignored		●		Visual/contrast by Inspection standard film
			$Y \leq 1/4L \quad X \leq 5 \quad Z \leq 1/2T$	2				
			$Y \leq 1/3L \quad X \leq 5 \quad Z \leq 1/2T$	1				
			$Y \leq 1/3L \quad X \leq 10 \quad Z \leq 1/2T$	0				
			$Y \leq 1/3L \quad X \leq 15 \quad Z \leq 1/2T$	0				
Crack			Cracks in any area	rejected		●		Visual
Polarizer			≤ 0.8	Accepted		●		Visual/

AQM0802A-RN-GBW(ZETTLER DISPLAYS) CHARACTER MODULE VER1.0

		be applicable for up/bottom polarizer	0.8<L≤1.0	Rejected			contrast by Inspection standard film
			1.0<L≤1.5	Rejected			
			1.5<L≤2.0	Rejected			
			<p>Any seeable polarizer slanting or excursion in active area will be rejected.</p> <p>The polarizer edge should be even and be line. Any indentation within 1/3 of silkscreen line will be rejected.</p> <p>Wrong direction, missing or extra, incorrect sticking for polarizer and dirty surface(grease) on polarizer will be rejected.</p> <p>seeable black silkscreen line from the arond can be accepted.</p> <p>Refer to the drawing size requirement.</p>				
End seal		 <p>L:The distance from the block to edge of glass.</p>	UV glue of seal on the glass surface	Rejected	●		Visual/contrast by Inspection standard film
			The UV glue of seal overflow into the active area.	Rejected			
			Direction of end seal is different from the drawing.	Rejected			
			Glue capacity of end seal < (1/3)*L	Rejected			
			the height and length of end seal is out of the drawing requirements.	Rejected			
Silkscreen line			silkscreen line overflow into the active area.	Rejected	●		Visual/contrast by Inspection standard film
			silkscreen line deviated in active area.	Rejected			
			bubble of silkscreen line ≥ 1/3 width of silkscreen line	Rejected			

AQM0802A-RN-GBW(ZETTLER DISPLAYS) CHARACTER MODULE VER1.0

PIN			<p>Glue on PIN: there is glue on the PIN without pin clip will be rejected. PIN glue solidification: PIN glue doesn't solidify completely. The sunken or glue stain by touching will be rejected.</p> <p>PIN deflection: if deflection angle $> \pm 5^\circ$, rejected; contrarily, please refer to the drawing requirement. Without continuous glue on pins will be rejected.</p> <p>PIN glue stains on polarizer or inleakage polarizer and glass, rejected.</p> <p>PIN glue exceeds the up polarizer, rejected.</p> <p>Missing or extra, broken pin, rejected.</p> <p>PIN loosen: no permission for pin loose or drop. Clip</p> <p>PIN:pin center exceeds 1/3 ITO width, rejected. No pin glue, rejected. UV glue range: UV glue must be exceeded over 1~1.5 pin distance from both side. if not, rejected. PIN length and direction must be same with the drawing requirements.</p>		●	Visual/ contrast by Inspection standard film	
Protective film			<p>LCD protective film can not stick on the polarizer and the product protective film raised $\leq 1/3$ length or width of polarizer from same direction of axis and its total length should be $\leq 15\text{mm}$. This defect can be accepted.</p>		●	Visual	
Rainbow			rainbow is not in active area.	Accepted		●	Visual/co ntrast by golden sample
			Rainbow in active area.	Rejected			
			with obvious discoloration and uneven color.	Rejected			
backgroud color			There are obvious different background color from the same product lot.	Rejected		●	Visual/co ntrast by golden sample

NOTE:

Inspection condition:

Viewing distance for cosmetic inspection is 30cm with bare eyes, and under an environment of 800 lux(20W*2---40W) light intensity, all directions for inspecting the sample should be within 45° against perpendicular

15.0 PRECAUTION FOR USING LCM

1. When design the product with this LCD Module, make sure the viewing angle matches to its purpose of usage.
2. As LCD panel is made of glass substrate, Dropping the LCD module or banging it against hard objects may cause cracking or fragmentation. Especially at corners and edges.
3. Although the polarizer of this LCD Module has the anti-glare coating, always be careful not to scratch its surface. Use of a plastic cover is recommended to protect the surface of polarizer.
4. If the LCD module is stored at below specified temperature, the LC material may freeze and be deteriorated. If it is stored at above specified temperature, the molecular orientation of the LC material may change to Liquid state and it may not revert to its original state. Excessive temperature and humidity could cause polarizer peel off or bubble. Therefore, the LCD module should always be stored within specified temperature range.
5. Saliva or water droplets must be wiped off immediately as those may leave stains or cause color changes if remained for a long time. Water vapor will cause corrosion of ITO electrodes.
6. If the surface of LCD panel needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If it is not still clean enough, blow a breath on the surface and wipe again.
7. The module should be driven according to the specified ratings to avoid malfunction and permanent damage. Applying DC voltage cause a rapid deterioration of LC material. Make sure to apply alternating waveform by continuous application of the M signal. Especially the power ON/OFF sequence should be kept to avoid latch-up of driver LSIs and DC charge up to LCD panel.
8. Mechanical Considerations
 - a) LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
 - b) Do not tamper in any way with the tabs on the metal frame.
 - c) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
 - d) Do not touch the elastomer connector; especially insert a backlight panel (for example, EL).
 - e) When mounting a LCM makes sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
 - f) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
9. Static Electricity
 - a) Operator

Wear the electrostatics shielded clothes because human body may be statically charged if not wear shielded clothes. Never touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

b) Equipment

There is a possibility that the static electricity is charged to the equipment, which has a function of peeling or friction action (ex: conveyer, soldering iron, working table). Earth the equipment through proper resistance (electrostatic earth: 1×10^8 ohm).

Only properly grounded soldering irons should be used.

If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

c) Floor

Floor is the important part to drain static electricity, which is generated by operators or equipment.

There is a possibility that charged static electricity is not properly drained in case of insulating floor. Set the electrostatic earth (electrostatic earth: 1×10^8 ohm).

d) Humidity

Proper humidity helps in reducing the chance of generating electrostatic charges. Humidity should be kept over 50%RH.

e) Transportation/storage

The storage materials also need to be anti-static treated because there is a possibility that the human body or storage materials such as containers may be statically charged by friction or peeling.

The modules should be kept in antistatic bags or other containers resistant to static for storage.

f) Soldering

Solder only to the I/O terminals. Use only soldering irons with proper grounding and no leakage.

Soldering temperature : $280^{\circ} \text{C} \pm 10^{\circ} \text{C}$

Soldering time: 3 to 4 sec.

Use eutectic solder with resin flux fill.

AQM0802A-RN-GBW(ZETTLER DISPLAYS) CHARACTER MODULE VER1.0

If flux is used, the LCD surface should be covered to avoid flux splatters. Flux residue should be removed afterwards.

g) Others

The laminator (protective film) is attached on the surface of LCD panel to prevent it from scratches or stains. It should be peeled off slowly using static eliminator.

Static eliminator should also be installed to the workbench to prevent LCD module from static charge.

10. Operation

- a) Driving voltage should be kept within specified range; excess voltage shortens display life.
 - b) Response time increases with decrease in temperature.
 - c) Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".
 - d) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".
11. If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. The toxicity is extremely low but caution should be exercised at all the time.
 12. Disassembling the LCD module can cause permanent damage and it should be strictly avoided.
 13. LCD retains the display pattern when it is applied for long time (Image retention). To prevent image retention, do not apply the fixed pattern for a long time. Image retention is not a deterioration of LCD. It will be removed after display pattern is changed.
 14. Do not use any materials, which emit gas from epoxy resin (hardener for amine) and silicone adhesive agent (dealcohol or deoxym) to prevent discoloration of polarizer due to gas.
 15. Avoid the exposure of the module to the direct sunlight or strong ultraviolet light for a long time.